

6,069,021

6,475,882-3

20/403, 864

Examiner's Notes

Requested written restriction

S(epitax, or crystal?)

S(CuN or gallium(IV) nitride)

S(substrate?)

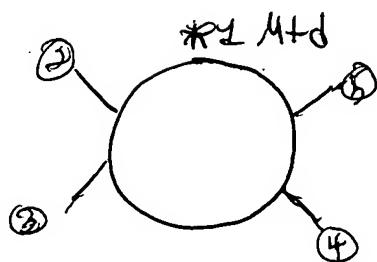
S(single or mono) (8a) (crystal)

(S(Boron) phosphite(w) buffer or Boron(IV) phosphite)

(S(layer #)

S(first or primary) (4a) (layer)

S(second?) (4b) (layer#)



Motivation: In order to provide a process & epitaxial structure
of Cu-N-based compd SC which discloses a process for growing
a buffer layer composed of Cu-N-based at a low/high
temperature during one process for an epitaxial layer w/ perfect lattice

8.08. 1) [S-I-S are]

2) [An epitaxial structure of GaN]

Prob

3) [423]

4) [3282]

5) [Sb-10 are]

6) [A process of epitaxial structure of GaN]

Mtd

7) [117]

8) [84+]

A III-V compound SC such as GaP, GaAs, or BP

Udagawa et al. feather a BP Based SC comprising

Search History

=> d 112 1-33 abs,bib

STN

(HCAPLUS, INPDOC, STN, USPATFULL, INPADOC)
20/05

10/714, 612
10/689, 024
10/825, 498
(6) 831, 293
(6) 831, 408
(6) 831, 304
(6) 730, 941
(6) 825, 962
(6) 809, 346

L12 ANSWER 1 OF 33 HCAPLUS COPYRIGHT 2005 ACS on STN
AB The present invention relates to a process and **epitaxial** structure of semiconductor and, more particularly, to a process and **epitaxial** structure of GaN based compound semiconductor which includes a buffer layer of Group III nitride formed on a **single crystal of boron phosphide** by growing a **first layer** at a low temperature and a **second layer** at a high temperature for growing a lattice-matched structure. The **epitaxial** structure of GaN based compound semiconductor comprises a **substrate**; a **single crystal of B phosphide buffer layer** on the **substrate**; a 1st **buffer layer** composed of Group III nitride at a temperature of 200-800° formed on the B phosphide buffer layer; and a 2nd **buffer layer** composed of Group III nitride at a temperature of 800° formed on the 1st **buffer layer**.

AN 2005:717 HCAPLUS

DN 142:104388

TI **Epitaxial structure and process of growing GaN-based compound semiconductors**

IN Lai, Mu Jen; Chang, Chiung Yu; Liu, Chia Cheng

PA Taiwan

SO U.S. Pat. Appl. Publ., 8 pp
CODEN: USXXCO

DT Patent

LA English

FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2004261693	A1	20041230	US 2003-603864	20030626
PRAI US 2003-603864		20030626		

L12 ANSWER 2 OF 33 INPADOC COPYRIGHT 2005 EPO on STN

LEVEL 1

AN 252096567 INPADOC ED 20050113 EW 200502 UP 20050331 UW 200513

TI **Epitaxial structure and process of GaN based compound semiconductor.**

IN LAI MU JEN; CHANG CHIUNG YU; LIU CHIA CHENG

INS LAI MU JEN; CHANG CHIUNG YU; LIU CHIA CHENG

INA TW; TW; TW

PA LAI MU JEN; CHANG CHIUNG YU; LIU CHIA CHENG

PAS LAI MU JEN; CHANG CHIUNG YU; LIU CHIA CHENG

PAA TW; TW; TW

TL English

DT Patent

PIT USAA PATENT APPLICATION PUBLICATION (PRE-GRANT)

PI US 2004261693 AA 20041230

AI US 2003-603864 A 20030626

PRAI US 2003-603864 A 20030626 (EDBR 20050113)

L12 ANSWER 3 OF 33 USPATFULL on STN

AB An **epitaxial** structure of GaN based compound semiconductor comprises a **substrate**; a **single crystal of boron phosphide buffer layer** on the **substrate**; a **first buffer layer** composed of group III nitride at a temperature from 200 to 800 degree C. formed on the **boron phosphide buffer layer**; and a **second buffer layer** composed of group III nitride at a temperature from 800 degree formed on the **first buffer layer**.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:330625 USPATFULL

TI **Epitaxial structure and process of GaN based**

IN compound semiconductor
Lai, Mu Jen, Hsin Chu, TAIWAN, PROVINCE OF CHINA
Chang, Chiung Yu, Hsin Chu, TAIWAN, PROVINCE OF CHINA
Liu, Chia Cheng, Hsin Chu, TAIWAN, PROVINCE OF CHINA

PI US 2004261693 A1 20041230
AI US 2003-603864 A1 20030626 (10)

DT Utility

FS APPLICATION

LREP ROSENBERG, KLEIN & LEE, 3458 ELLICOTT CENTER DRIVE-SUITE 101, ELLICOTT CITY, MD, 21043

CLMN Number of Claims: 10

ECL Exemplary Claim: 1

DRWN 5 Drawing Page(s)

LN.CNT 215

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 4 OF 33 USPATFULL on STN

AB The present invention provides a technique for fabricating a multicolor light-emitting lamp by using a blue LED having a structure capable of avoiding cumbersome bonding. In particular, the present invention provides a technique for fabricating a multicolor light-emitting lamp by using a hetero-junction type GaP-base LED capable of emitting high intensity green light in combination. Also, for example, in fabricating a multicolor light-emitting lamp from the blue LED and the yellow LED, the present invention provides a technique for fabricating a multicolor light-emitting lamp from a blue LED requiring no cumbersome bonding and a hetero-junction type GaAs._{1-ZP}._Z-base yellow LED of emitting light having high light emission intensity.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:237290 USPATFULL

TI Multicolor light-emitting lamp and light source

IN Udagawa, Takashi, Chichibu-shi, JAPAN

PI US 2004183089 A1 20040923

AI US 2004-486985 A1 20040218 (10)
WO 2002-JP8317 20020816

PRAI JP 2001-248455 20010820

US 2001-323088P 20010919 (60)

DT Utility

FS APPLICATION

LREP Sughrue Mion, 2100 Pennsylvania Avenue NW, Washington, DC, 20037-3213

CLMN Number of Claims: 6

ECL Exemplary Claim: 1

DRWN 4 Drawing Page(s)

LN.CNT 872

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 5 OF 33 USPATFULL on STN

AB The present invention discloses a light emitting diode (LED) by using a P-type ZnTe layer or a ZnSe layer as a substrate. To match the lattice between the substrate and blue light LED of cubic crystal, a BP(boron phosphide) buffer layer of single crystal is formed on the substrate. When the blue light LED emits blue light of wavelength from 450 nm to 470 nm, the ZnTe or ZnSe substrate absorbs the blue light and emits yellow-green light of wavelength 550 nm. Thus, white light is produced by mixing the blue light and the yellow-green light.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:225422 USPATFULL

TI WHITE LIGHT LED

IN Lai, Mu-Jen, Hsinchu, TAIWAN, PROVINCE OF CHINA

Liu, Chia-Cheng, Hsinchu, TAIWAN, PROVINCE OF CHINA

Chang, Chiung-Yu, Hsinchu, TAIWAN, PROVINCE OF CHINA

PI US 2004173805 A1 20040909

* US 6825498 B2 20041130

AI US 2003-603659 A1 20030626 (10)

PRAI TW 2003-92104599 20030304
DT Utility
FS APPLICATION
LREP RABIN & Berdo, PC, 1101 14TH STREET, NW, SUITE 500, WASHINGTON, DC,
20005
CLMN Number of Claims: 10
ECL Exemplary Claim: 1
DRWN 2 Drawing Page(s)
LN.CNT 333

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 6 OF 33 USPATFULL on STN

AB A boron-phosphide-based semiconductor light-emitting device having a semiconductor substrate of a first conduction type having, on its bottom surface, a bottom electrode; a first boron-phosphide-based semiconductor layer of a first conductive type provided on the substrate; a Group III-V compound semiconductor active layer provided on the first boron-phosphide-based semiconductor layer; a second boron-phosphide-based semiconductor layer of second conduction type provided on the active layer; and a top electrode provided on the surface of the second boron-phosphide-based semiconductor layer. The top electrode includes a lower electrode and an upper electrode, the lower electrode is in direct contact with the second boron-phosphide-based semiconductor layer and formed of a metal incapable of establishing ohmic contact with the second boron-phosphide-based semiconductor layer, and the upper electrode is provided on the lower electrode and formed of a metal capable of establishing ohmic contact with the second boron-phosphide-based semiconductor layer.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:219431 USPATFULL
TI BORON PHOSPHIDE-BASED SEMICONDUCTOR LIGHT-EMITTING DEVICE, PRODUCTION METHOD THEREOF, AND LIGHT-EMITTING DIODE
IN Udagawa, Takashi, Saitama, JAPAN
PA SHOWA DENKO K.K. (non-U.S. corporation)
PI US 2004169191 A1 20040902
US 6809346 B2 20041026
AI US 2004-795302 A1 20040309 (10)
RLI Continuation of Ser. No. US 2003-353006, filed on 29 Jan 2003, GRANTED,
Pat. No. US 6730941
PRAI JP 2002-20824 20020130
US 2002-384097P 20020531 (60)
DT Utility
FS APPLICATION
LREP SUGHRUE MION, PLLC, 2100 PENNSYLVANIA AVENUE, N.W., SUITE 800,
WASHINGTON, DC, 20037
CLMN Number of Claims: 20
ECL Exemplary Claim: 1
DRWN 3 Drawing Page(s)
LN.CNT 893

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 7 OF 33 USPATFULL on STN

AB A boron phosphide-based semiconductor light-emitting device, which device includes a light-emitting member having a hetero-junction structure in which an n-type lower cladding layer formed of an n-type compound semiconductor, an n-type light-emitting layer formed of an n-type Group III nitride semiconductor, and a p-type upper cladding layer provided on the light-emitting layer and formed of a p-type boron phosphide-based semiconductor are sequentially provided on a surface of a conductive or high-resistive single-crystal substrate and which device includes a p-type Ohmic electrode provided so as to achieve contact with the p-type upper

cladding layer, characterized in that a amorphous layer formed of boron phosphide-based semiconductor is disposed between the p-type upper cladding layer and the n-type light-emitting layer. This boron phosphide-based semiconductor light-emitting device exhibits a low forward voltage or threshold value and has excellent reverse breakdown voltage characteristics.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:219424 USPATFULL
TI Boron phosphide-based semiconductor light-emitting device, production method thereof and light-emitting diode
IN Udagawa, Takashi, Chichibu-shi, JAPAN
Kasahara, Akira, Chichibu-shi, JAPAN
PA SHOWA DENKO K.K. (non-U.S. corporation)
PI US 2004169184 A1 20040902
AI US 2003-714612 A1 20031118 (10)
PRAI JP 2002-333208 20021118
JP 2002-369577 20021220
JP 2002-370420 20021220
US 2002-428716P 20021125 (60)
US 2002-436640P 20021230 (60)
US 2002-436641P 20021230 (60)
DT Utility
FS APPLICATION
LREP SUGHRUE MION, PLLC, 2100 PENNSYLVANIA AVENUE, N.W., SUITE 800,
WASHINGTON, DC, 20037
CLMN Number of Claims: 23
ECL Exemplary Claim: 1
DRWN 4 Drawing Page(s)
LN.CNT 1930

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 8 OF 33 USPATFULL on STN

AB A light-emitting device with reduced lattice mismatch. The light-emitting device comprises a substrate having a first lattice constant, a first buffer multilayer deposited on the substrate, a second buffer multilayer deposited on the first buffer multilayer, and a GaN base epitaxial layer deposited on the second buffer multilayer. The lattice constant of the first buffer multilayer ranges from the first lattice constant at the bottom of the first buffer multilayer to a second lattice constant at the top of the first buffer multilayer. The lattice constant of the second buffer multilayer ranges from the second lattice constant at the bottom of the second buffer multilayer to a third lattice constant at the top of the second buffer multilayer.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:148943 USPATFULL
TI Light-emitting device with reduced lattice mismatch
IN Lai, Mu-Jen, Jungli City, TAIWAN, PROVINCE OF CHINA
Chang, Chiung-Yu, Hsinchu, TAIWAN, PROVINCE OF CHINA
PI US 2004113155 A1 20040617
US 6815722 B2 20041109
AI US 2003-601957 A1 20030623 (10)
PRAI TW 2002-91136160 20021213
DT Utility
FS APPLICATION
LREP THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP, 100 GALLERIA PARKWAY, NW, STE
1750, ATLANTA, GA, 30339-5948
CLMN Number of Claims: 9
ECL Exemplary Claim: 1
DRWN 2 Drawing Page(s)
LN.CNT 391

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 9 OF 33 USPATFULL on STN

AB A Group-III nitride semiconductor device including a crystal

substrate, an electrically conducting Group-III nitride semiconductor (Al_xGa_yIn_zN: 0≤x<1, 0<y≤1 and 0<x+y≤1) **crystal layer** vapor-phase grown on the **crystal substrate**, an ohmic electrode and an electrically conducting boron phosphide **crystal layer** provided between the ohmic electrode and the Group-III nitride semiconductor **crystal layer**, the ohmic electrode being disposed in contact with the boron phosphide **crystal layer**. Also disclosed is a method for producing the Group-III nitride semiconductor device, and a light-emitting diode including the Group-III nitride semiconductor device.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:105570 USPATFULL
TI Group-III nitride semiconductor device, production method thereof and light-emitting diode
IN Udagawa, Takashi, Saitama, JAPAN
PA SHOWA DENKO K.K. (non-U.S. corporation)
PI US 2004079959 A1 20040429
AI US 2003-689024 A1 20031021 (10)
PRAI JP 2002-306722 20021022
US 2002-422121P 20021030 (60)
DT Utility
FS APPLICATION
LREP SUGHRUE MION, PLLC, 2100 PENNSYLVANIA AVENUE, N.W., SUITE 800,
WASHINGTON, DC, 20037
CLMN Number of Claims: 18
ECL Exemplary Claim: 1
DRWN 2 Drawing Page(s)
LN.CNT 756

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 10 OF 33 USPATFULL on STN

AB A semiconductor device is prepared by the use of a vapor phase method and is provided with a semiconductor **layer** composed of **boron phosphide (BP)** having a band gap at room temperature of not less than 2.8 eV and not more than 3.4 eV or a **boron phosphide (BP)-base mixed crystal** which contains the **boron phosphide (BP)** and which is represented by the formula:

B_{sub.α}Al_{sub.β}Ga_{sub.γ}In_{sub.1-α-β-γ}P_{sub.δ}As_{sub.ε}N_{sub.1-δ-ε}
(0<α=1, 0=β<1, 0=γ<1, 0<α+β+γ=1,
0<δ=1, 0=ε<1, 0<δ+ε=1).

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:333532 USPATFULL
TI Semiconductor device, semiconductor **layer** and production method thereof
IN Udagawa, Takashi, Chichibu-shi, JAPAN
PI US 2003234400 A1 20031225
AI US 2003-332200 A1 20030107 (10)
WO 2002-JP5007 20020523
PRAI JP 2001-158282 20010528
DT Utility
FS APPLICATION
LREP SUGHRUE MION, PLLC, 2100 PENNSYLVANIA AVENUE, N.W., WASHINGTON, DC,
20037
CLMN Number of Claims: 11
ECL Exemplary Claim: 1
DRWN 9 Drawing Page(s)
LN.CNT 1797

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 11 OF 33 USPATFULL on STN

AB A method of forming a group-III nitride semiconductor **layer** on

a light-emitting device. First, a **substrate** is provided. Next, a **buffer layer** is formed on the **substrate**. A hydrogen treatment is performed on the **buffer layer**. Finally, a group-III nitride semiconductor **layer** is formed on the **buffer layer**. According to the present invention, a hydrogen treatment is performed on the buffer to prevent corrosion during subsequent process and remove particles from the **buffer layer**. Thus, the structure of the **epitaxy layer** following formed on the **buffer layer** is enhanced.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003-318803 USPATFULL
TI Method of forming group-III nitride semiconductor **layer** on a light-emitting device
IN Terashima, Kazutaka, Hsinchu, TAIWAN, PROVINCE OF CHINA
Lai, Mu-Jen, Chuagli City, TAIWAN, PROVINCE OF CHINA
Chang, Chiung-Yu, Taichung, TAIWAN, PROVINCE OF CHINA
PI US 2003224548 A1 20031204
US 6828169 B2 20041207
AI US 2003-463355 A1 20030617 (10)
RLI Continuation-in-part of Ser. No. US 2002-62116, filed on 30 Jan 2002,
PENDING
PRAI TW 2002-91120763 20020911
DT Utility
FS APPLICATION
LREP THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP, 100 GALLERIA PARKWAY, NW, STE
1750, ATLANTA, GA, 30339-5948
CLMN Number of Claims: 20
ECL Exemplary Claim: 1
DRWN 3 Drawing Page(s)
LN.CNT 302

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 12 OF 33 USPATFULL on STN

AB A p-n junction-type compound semiconductor light-emitting device having a **substrate** formed of a **single crystal**, a **first barrier layer** provided on the **substrate** and formed of a compound semiconductor of a first conduction type, a **light-emitting layer** provided on the **first barrier layer** and formed of an indium (In)-containing group III nitride semiconductor of a first or a second conduction type, and an **evaporation-preventing layer** provided on the **light-emitting layer** for preventing the evaporation of indium from the **light-emitting layer**. The **evaporation-preventing layer** is formed of an undoped **boron phosphide (BP)**-base semiconductor of a second conduction type. A method for producing the semiconductor-light emitting device is also disclosed.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003-255589 USPATFULL
TI P-n junction-type compound semiconductor light-emitting device, production method thereof, lamp and light source
IN Udagawa, Takashi, Saitama, JAPAN
PA SHOWA DENKO K.K. (non-U.S. corporation)
PI US 2003178631 A1 20030925
US 6831293 B2 20041214
AI US 2003-389904 A1 20030318 (10)
PRAI JP 2002-75297 20020319
US 2002-384095P 20020531 (60)
DT Utility
FS APPLICATION
LREP SUGHRUE MION, PLLC, 2100 PENNSYLVANIA AVENUE, N.W., WASHINGTON, DC,
20037
CLMN Number of Claims: 13
ECL Exemplary Claim: 1
DRWN 4 Drawing Page(s)
LN.CNT 956

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 13 OF 33 USPATFULL on STN

AB A pn-junction type compound semiconductor light-emitting device having a substrate formed of a crystal, a first barrier layer provided on the substrate and formed of an undoped boron phosphide-base semiconductor of first conduction type, and a light-emitting layer of a first or a second conduction type provided on the first barrier layer including a plurality of superposed constituent layers formed of group III nitride semiconductors each having a different band gap. The constituent layer of the light-emitting layer provided closest to the first barrier layer is a first light-emitting constituent layer formed of a group III nitride semiconductor containing phosphorus (P). A method for producing the semiconductor light-emitting device is also disclosed.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:248793 USPATFULL

TI Pn-junction type compound semiconductor light-emitting device, production method thereof and white light-emitting diode

IN Udagawa, Takashi, Saitama, JAPAN

PA SHOWA DENKO K.K. (non-U.S. corporation)

PI US 2003173573 A1 20030918

US 6774402 B2 20040810

AI US 2003-384666 A1 20030311 (10)

PRAI JP 2002-67473 20020312

US 2002-430648P 20021204 (60)

DT Utility

FS APPLICATION

LREP SUGHRUE MION, PLLC, 2100 PENNSYLVANIA AVENUE, N.W., WASHINGTON, DC, 20037

CLMN Number of Claims: 13

ECL Exemplary Claim: 1

DRWN 3 Drawing Page(s)

LN.CNT 1252

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 14 OF 33 USPATFULL on STN

AB A pn-junction-type boron-phosphide-based semiconductor light-emitting device having a single-crystal silicon (Si) substrate of first conduction type; a first boron-phosphide-based semiconductor layer of first conduction type provided on the substrate; a light-emitting layer formed of a Group III-V semiconductor layer of first or second conduction type which is doped with an element belonging to Group IV of the periodic table provided on the first boron-phosphide-based semiconductor layer; and second boron-phosphide-based semiconductor layer of second conduction type formed of a boron-phosphide-based semiconductor layer of second conduction type containing a Group IV element provided on the light-emitting layer. The first boron-phosphide-based semiconductor layer, the light-emitting layer, and the second boron-phosphide-based semiconductor layer form a pn-junction-type hetero structure. In addition, the second conduction type is opposite the first conduction type. Also, disclosed is a method for producing the device.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:230061 USPATFULL

TI P-n junction type boron phosphide-based semiconductor light-emitting device and production method thereof

IN Udagawa, Takashi, Saitama, JAPAN

PA SHOWA DENKO K.K. (non-U.S. corporation)

PI US 2003160253 A1 20030828

on the cladding layer. The barrier layer is formed from a boron-containing Group III-V compound semiconductor having the same lattice constant as a boron-containing Group III-V compound semiconductor constituting the cladding layer.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:37454 USPATFULL
TI Stacked layer structure, light-emitting device, lamp, and light source unit
IN Udagawa, Takashi, Saitama, JAPAN
PA SHOWA DENKO K.K. (non-U.S. corporation)
PI US 2003027099 A1 20030206
US 6835962 B2 20041228
AI US 2002-207901 A1 20020731 (10)
PRAI JP 2001-233428 20010801
JP 2001-235454 20010802
JP 2001-247523 20010817
US 2001-311103P 20010810 (60)
US 2001-311073P 20010810 (60)
US 2001-323084P 20010919 (60)

DT Utility

FS APPLICATION

LREP SUGHRUE MION, PLLC, 2100 PENNSYLVANIA AVENUE, N.W., WASHINGTON, DC, 20037

CLMN Number of Claims: 13

ECL Exemplary Claim: 1

DRWN 3 Drawing Page(s)

LN.CNT 1177

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 17 OF 33 USPATFULL on STN

AB A method of growing a group III nitride semiconductor crystal layer includes a step of growing a first buffer layer composed of boron phosphide on a silicon single crystal substrate by a vapor phase growth method at a temperature of not lower than 200° C. and not higher than 700° C., a step of growing a second buffer layer composed of boron phosphide on the first buffer layer by a vapor phase growth method at a temperature of not lower than 750° C. and not higher than 1200° C., and a step of growing a crystal layer composed of group III nitride semiconductor crystal represented by general formula Al_p.sub.q Ga_r.sub.q In_r.sub.p N (where 0≤p≤1, 0≤q≤1, 0≤r≤1, p+q+r=1) on the second buffer layer by a vapor phase growth method. A semiconductor device incorporating the group III nitride semiconductor crystal layer is provided.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2001:29894 USPATFULL

TI Method of growing group III nitride semiconductor crystal layer and semiconductor device incorporating group III nitride semiconductor crystal layer

IN Udagawa, Takashi, Chichibu, Japan
Terashima, Kazutaka, Ebina, Japan
Nishimura, Suzuka, Yamaguchi, Japan
Tsuzaki, Takuji, Matsumoto, Japan

PA Showa Denko Kabushiki Kaisha, Tokyo, Japan (non-U.S. corporation)

PI US 6194744 B1 20010227

AI US 2000-500450 20000209 (9)

RLI Division of Ser. No. US 1999-270749, filed on 17 Mar 1999, now patented, Pat. No. US 6069021

PRAI JP 1998-66769 19980317
JP 1999-36830 19990216

DT Utility

FS Granted

EXNAM Primary Examiner: Chaudhuri, Olik; Assistant Examiner: Wille, Douglas A.

AI US 6831304 B2 20041214
PRAI US 2003-370761 A1 20030224 (10)
JP 2002-47457 20020225
US 2002-367702P 20020328 (60)
DT Utility
FS APPLICATION
LREP SUGHRUE MION, PLLC, 2100 PENNSYLVANIA AVENUE, N.W., WASHINGTON, DC,
20037
CLMN Number of Claims: 12
ECL Exemplary Claim: 1
DRWN 2 Drawing Page(s)
LN.CNT 1278
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 15 OF 33 USPATFULL on STN
AB A **boron-phosphide**-based semiconductor light-emitting device having a semiconductor **substrate** of a first conduction type having, on its bottom surface, a bottom electrode; a **first boron-phosphide**-based semiconductor **layer** of a first conductive type provided on the **substrate**; a Group III-V compound semiconductor active **layer** provided on the **first boron-phosphide**-based semiconductor **layer**; a **second boron-phosphide**-based semiconductor **layer** of second conduction type provided on the active **layer**; and a top electrode provided on the surface of the **second boron-phosphide**-based semiconductor **layer**. The top electrode includes a lower electrode and an upper electrode, the lower electrode is in direct contact with the **second boron-phosphide**-based semiconductor **layer** and formed of a metal incapable of establishing ohmic contact with the **second boron-phosphide**-based semiconductor **layer**, and the upper electrode is provided on the lower electrode and formed of a metal capable of establishing ohmic contact with the **second boron-phosphide**-based semiconductor **layer**.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:205162 USPATFULL
TI **Boron phosphide**-based semiconductor light-emitting device, production method thereof, and light-emitting diode
IN Udagawa, Takashi, Saitama, JAPAN
PA SHOWA DENKO K.K. (non-U.S. corporation)
PI US 2003141509 A1 20030731
US 6730941 B2 20040504
AI US 2003-353006 A1 20030129 (10)
PRAI JP 2002-20824 20020130
US 2002-384097P 20020531 (60)
DT Utility
FS APPLICATION
LREP SUGHRUE MION, PLLC, 2100 PENNSYLVANIA AVENUE, N.W., WASHINGTON, DC,
20037
CLMN Number of Claims: 15
ECL Exemplary Claim: 1
DRWN 3 Drawing Page(s)
LN.CNT 845

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 16 OF 33 USPATFULL on STN
AB A stacked layer structure including a **single crystal substrate**; an amorphous or polycrystalline **buffer layer** formed from a boron-containing Group III-V compound semiconductor. The **buffer layer** is provided on the **substrate**; a cladding **layer** formed from a boron-containing Group III-V compound semiconductor is provided on the **buffer layer**; and a light-emitting **layer** having a quantum well structure including a barrier **layer** formed from a boron-containing Group III-V compound semiconductor and a well **layer** formed from a Group III nitride semiconductor is provided

LREP Sughrue, Mion, Zinn, Macpeak & Seas, PLLC

CLMN Number of Claims: 6

ECL Exemplary Claim: 1

DRWN 3 Drawing Figure(s); 3 Drawing Page(s)

LN.CNT 959

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 18 OF 33 USPATFULL on STN

AB A method of growing a group III nitride semiconductor **crystal layer** includes a step of growing a **first buffer layer** composed of **boron phosphide** on a **silicon single crystal substrate** by a vapor phase growth method at a temperature of not lower than 200° C. and not higher than 700° C., a step of growing a **second buffer layer** composed of **boron phosphide** on the **first buffer layer** by a vapor phase growth method at a temperature of not lower than 750° C. and not higher than 1200° C., and a step of growing a **crystal layer** composed of group III nitride semiconductor **crystal** represented by general formula Al_pGa_{1-p}In_rN (where 0≤p≤1, 0≤q≤1, 0≤r≤1, p+q+r=1) on the **second buffer layer** by a vapor phase growth method. A semiconductor device incorporating the group III nitride semiconductor **crystal layer** is provided.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2000:67610 USPATFULL

TI Method of growing group III nitride semiconductor **crystal layer** and semiconductor device incorporating group III nitride semiconductor **crystal layer**

IN Terashima, Kazutaka, Ebina, Japan
Nishimura, Suzuka, Yamaguchi, Japan
Tsuzaki, Takuji, Matsumoto, Japan
Udagawa, Takashi, Chichibu, Japan

PA Showa Denko K.K., Tokyo, Japan (non-U.S. corporation)

US 6069021 20000530

AI US 1999-270749 19990317 (9)

PRAI JP 1998-66769 19980317
JP 1998-180921 19980626
JP 1998-193125 19980708
JP 1998-232279 19980806
JP 1999-36830 19990216
US 1999-119326P 19990209 (60)

DT Utility

FS Granted

EXNAME Primary Examiner: Chaudhuri, Olik; Assistant Examiner: Wille, Douglas A.

LREP Sughrue, Mion, Zinn, Macpeak & Seas, PLLC

CLMN Number of Claims: 10

ECL Exemplary Claim: 1

DRWN 3 Drawing Figure(s); 3 Drawing Page(s)

LN.CNT 988

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 19 OF 33 USPATFULL on STN

AB A semiconductor device comprises a **single crystal substrate**, a nucleus formation **buffer layer** formed on the **single crystal substrate**, and a **lamination layer** including a plurality of Al_{1-x-y}Ga_xIn_yN (0≤x≤1, 0≤y≤1, x+y≤1) **layers** laminated above the nucleus formation **buffer layer**. The nucleus formation **buffer layer** is formed of Al_{1-s-t}Ga_sIn_tN (0≤s≤1, 0≤t≤1, s+t≤1) and is formed on a surface of the **substrate** such that the nucleus formation **buffer layer** has a number of pinholes for control of polarity and formation of nuclei. A method of fabricating a semiconductor device comprises the steps of: forming, above an Al_{1-x-y}Ga_xIn_yN

($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x+y \leq 1$) semiconductor
layer doped with a p-type dopant, a cap layer for
preventing evaporation of a constituent element of the semiconductor
layer, the cap layer being formed of one of AlN in
which a p-type dopant is added and Al₁.sub.2 O₃.sub.3, subjecting the
semiconductor layer to heat treatment, and removing at least a
part of the cap layer.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 1999:85817 USPATFULL
TI Semiconductor device and method of fabricating the same
IN Ohba, Yasuo, Yokohama, Japan
Hatano, Ako, Tokyo, Japan
PA Kabushiki Kaisha Toshiba, Kawasaki, Japan (non-U.S. corporation)
PI US 5929466 19990727
AI US 1997-874299 19970613 (8)
RLI Continuation of Ser. No. US 1995-400865, filed on 8 Mar 1995, now
patented, Pat. No. US 5656832
PRAI JP 1994-38157 19940309
JP 1995-704 19950106
DT Utility
FS Granted
EXNAM Primary Examiner: Jackson, Jr., Jerome
LREP Oblon, Spivak, McClelland, Maier & Neustadt, P.C.
CLMN Number of Claims: 10
ECL Exemplary Claim: 1
DRWN 18 Drawing Figure(s); 6 Drawing Page(s)
LN.CNT 969

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 20 OF 33 USPATFULL on STN

AB A semiconductor device comprises a **single crystal substrate**, a nucleus formation buffer layer formed on the **single crystal substrate**, and a lamination layer including a plurality of Al₁.sub.1-x-y Ga_x.sub.y In₁.sub.y N ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x+y \leq 1$) layers laminated above the nucleus formation buffer layer. The nucleus formation buffer layer is formed of Al₁.sub.1-s-t Ga_s.sub.t In₁.sub.t N ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$) and formed on a surface of the **substrate** with an average film thickness of 5 nm to 20 nm such that the nucleus formation buffer layer has a number of pinholes for control of polarity and formation of nuclei. The pinholes are formed among loosely formed small **crystals** of Al₁.sub.1-s-t Ga_s.sub.t In₁.sub.t N ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$).

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 1999:63513 USPATFULL
TI Semiconductor device including quaternary buffer layer with
pinholes
IN Ohba, Yasuo, Yokohama, Japan
Hatano, Ako, Tokyo, Japan
PA Kabushiki Kaisha Toshiba, Kawasaki, Japan (non-U.S. corporation)
PI US 5909040 19990601
AI US 1997-866056 19970530 (8)
RLI Continuation-in-part of Ser. No. US 1995-400865, filed on 8 Mar 1995,
now patented, Pat. No. US 5656832
PRAI JP 1994-38157 19940309
JP 1995-704 19950106
DT Utility
FS Granted
EXNAM Primary Examiner: Jackson, Jr., Jerome
LREP Oblon, Spivak, McClelland, Maier & Neustadt, P.C.
CLMN Number of Claims: 15
ECL Exemplary Claim: 1
DRWN 19 Drawing Figure(s); 7 Drawing Page(s)
LN.CNT 1020

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 21 OF 33 USPATFULL on STN
AB Boron-aluminum nitride $B_{\text{sub.}x} Al_{\text{sub.}1-x} N_{\text{sub.}y}$
($0.001 \leq x \leq 0.70$, $0.85 \leq y \leq 1.05$) films having
wurtzite type structure are proposed. The material has higher hardness,
higher sound velocity and wider band gap than hexagonal aluminum nitride
(AlN).

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 1998:68710 USPATFULL
TI Boron-aluminum nitride coating and method of producing same
IN Utsumi, Yoshiharu, Itami, Japan
 Imai, Takahiro, Itami, Japan
 Fujimori, Naoji, Itami, Japan
PA Sumitomo Electric Industries Ltd., Osaka, Japan (non-U.S. corporation)
PI US 5766783 19980616
AI US 1995-565027 19951130 (8)
PRAI JP 1995-41687 19950301
 JP 1995-306899 19951030
DT Utility
FS Granted
EXNAM Primary Examiner: Speer, Timothy
LREP Pillsbury Madison & Sutro LLP
CLMN Number of Claims: 33
ECL Exemplary Claim: 1
DRWN 34 Drawing Figure(s); 6 Drawing Page(s)
LN.CNT 1580
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 22 OF 33 USPATFULL on STN

AB A semiconductor device comprises a **single crystal substrate**, a nucleus formation buffer **layer** formed on the **single crystal substrate**, and a **lamination layer** including a plurality of $Al_{\text{sub.}1-x-y} Ga_{\text{sub.}x} In_{\text{sub.}y} N$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x+y \leq 1$) **layers** laminated above the nucleus formation buffer **layer**. The nucleus formation buffer **layer** is formed of $Al_{\text{sub.}1-s-t} Ga_{\text{sub.}s} In_{\text{sub.}t} N$ ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$) and is formed on a surface of the **substrate** such that the nucleus formation buffer **layer** has a number of pinholes for control of polarity and formation of nuclei. A method of fabricating a semiconductor device comprises the steps of: forming, above an $Al_{\text{sub.}1-x-y} Ga_{\text{sub.}x} In_{\text{sub.}y} N$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x+y \leq 1$) semiconductor **layer** doped with a p-type dopant, a **cap layer** for preventing evaporation of a constituent element of the semiconductor **layer**, the **cap layer** being formed of one of AlN in which a p-type dopant is added and $Al_{\text{sub.}2} O_{\text{sub.}3}$, subjecting the semiconductor **layer** to heat treatment, and removing at least a part of the **cap layer**.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 97:71265 USPATFULL
TI Semiconductor heterojunction device with ALN buffer **layer** of 3nm-10nm average film thickness
IN Ohba, Yasuo, Yokohama, Japan
 Hatano, Ako, Tokyo, Japan
PA Kabushiki Kaisha Toshiba, Kawasaki, Japan (non-U.S. corporation)
PI US 5656832 19970812
AI US 1995-400865 19950308 (8)
PRAI JP 1994-38157 19940309
 JP 1995-704 19950106
DT Utility
FS Granted
EXNAM Primary Examiner: Jackson, Jerome
LREP Oblon, Spivak, McClelland, Maier & Neustadt, P.C.
CLMN Number of Claims: 12

ECL Exemplary Claim: 1
DRWN 18 Drawing Figure(s); 6 Drawing Page(s)
LN.CNT 969
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 23 OF 33 USPATFULL on STN

AB Solid layer semiconductor compositions are deposited by the simultaneous sputtering from a sputter target and electrically discharge a reacting gas preferably by application of an RF potential. Preferably, the method is used to make solid solution layers and most desirably solid solution epitaxial layers of at least two semiconductor materials. The method may be used to make novel metastable compositions such as (GaAs).sub.1.sub.-x Si.sub.x, (GaAs).sub.1.sub.-x Ge.sub.x, (InSb).sub.1.sub.-x Si.sub.x, (InSb).sub.1.sub.-x Ge.sub.x, (InAs).sub.1.sub.-x Si.sub.x and (InAs).sub.1.sub.-x Ge.sub.x (where x is a number greater than about 0.01, and $x + (1-x) = 1$, and Ga.sub.x As.sub.y Si.sub.z, Ga.sub.x As.sub.y Ge.sub.z, In.sub.x Sb.sub.y Si.sub.z, In.sub.x Sb.sub.y Ge.sub.z, In.sub.x As.sub.y Si.sub.z, In.sub.x As.sub.y Ge.sub.z and In.sub.x Sb.sub.y As.sub.z (where x, y and z are numbers greater than about 0.01, and $x + y + z = 1$).

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 76:49246 USPATFULL
TI Deposition of solid semiconductor compositions and novel semiconductor materials
IN Noreika, Alexander J., Pittsburgh, PA, United States
Francombe, Maurice H., Pittsburgh, PA, United States
PA Westinghouse Electric Corporation, Pittsburgh, PA, United States (U.S. corporation)
PI US 3979271 19760907
AI US 1973-381653 19730723 (5)
DT Utility
FS Granted
EXNAM Primary Examiner: Vertiz, Oscar R.; Assistant Examiner: Langel, Wayne A.
LREP Menzemer, C. L.
CLMN Number of Claims: 20
ECL Exemplary Claim: 1
DRWN 5 Drawing Figure(s); 3 Drawing Page(s)
LN.CNT 1379
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 24 OF 33 USPAT2 on STN

AB The present invention discloses a light emitting diode (LED) by using a P-type ZnTe layer or a ZnSe layer as a substrate. To match the lattice between the substrate and blue light LED of cubic crystal, a BP(boron phosphide) buffer layer of single crystal is formed on the substrate. When the blue light LED emits blue light of wavelength from 450 nm to 470 nm, the ZnTe or ZnSe substrate absorbs the blue light and emits yellow-green light of wavelength 550 nm. Thus, white light is produced by mixing the blue light and the yellow-green light.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:225422 USPAT2
TI White light LED
IN Lai, Mu-Jen, Hsinchu, TAIWAN, PROVINCE OF CHINA
Liu, Chia-Cheng, Hsinchu, TAIWAN, PROVINCE OF CHINA
Chang, Chiung-Yu, Hsinchu, TAIWAN, PROVINCE OF CHINA
PA Vtera Technology Inc., Hsinchu, TAIWAN, PROVINCE OF CHINA (non-U.S. corporation)
PI US 6825498 B2 20041130
AI US 2003-603659 20030626 (10)
PRAI TW 2003-92104599 20030304
DT Utility
FS GRANTED
EXNAM Primary Examiner: Ngo , Ngan V

LREP Rabin & Berdo, P.C.
CLMN Number of Claims: 10
ECL Exemplary Claim: 1
DRWN 3 Drawing Figure(s); 2 Drawing Page(s)
LN.CNT 333

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 25 OF 33 USPAT2 on STN

AB A boron-phosphide-based semiconductor light-emitting device having a semiconductor substrate of a first conduction type having, on its bottom surface, a bottom electrode; a first boron-phosphide-based semiconductor layer of a first conductive type provided on the substrate; a Group III-V compound semiconductor active layer provided on the first boron-phosphide-based semiconductor layer; a second boron-phosphide-based semiconductor layer of second conduction type provided on the active layer; and a top electrode provided on the surface of the second boron-phosphide-based semiconductor layer. The top electrode includes a lower electrode and an upper electrode, the lower electrode is in direct contact with the second boron-phosphide-based semiconductor layer and formed of a metal incapable of establishing ohmic contact with the second boron-phosphide-based semiconductor layer, and the upper electrode is provided on the lower electrode and formed of a metal capable of establishing ohmic contact with the second boron-phosphide-based semiconductor layer.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:219431 USPAT2

TI Boron phosphide-based semiconductor light-emitting device, production method thereof, and light-emitting diode

IN Udagawa, Takashi, Saitama, JAPAN

PA Showa Denko Kabushiki Kaisha, Tokyo, JAPAN (non-U.S. corporation)

PI US 6809346 B2 20041026

AI US 2004-795302 20040309 (10)

RLI Continuation of Ser. No. US 2003-353006, filed on 29 Jan 2003, now patented, Pat. No. US 6730941

PRAI JP 2002-20824 20020130

US 2002-384097P 20020531 (60)

DT Utility

FS GRANTED

EXNAM Primary Examiner: Hu, Shouxiang

LREP Sughrue Mion, PLLC

CLMN Number of Claims: 5

ECL Exemplary Claim: 1

DRWN 6 Drawing Figure(s); 3 Drawing Page(s)

LN.CNT 770

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 26 OF 33 USPAT2 on STN

AB A light-emitting device with reduced lattice mismatch. The light-emitting device comprises a substrate having a first lattice constant, a first buffer multilayer deposited on the substrate, a second buffer multilayer deposited on the first buffer multilayer, and a GaN base epitaxial layer deposited on the second buffer multilayer. The lattice constant of the first buffer multilayer ranges from the first lattice constant at the bottom of the first buffer multilayer to a second lattice constant at the top of the first buffer multilayer. The lattice constant of the second buffer multilayer ranges from the second lattice constant at the bottom of the second buffer multilayer to a third lattice constant at the top of the second buffer multilayer.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:148943 USPAT2

TI Light-emitting device with reduced lattice mismatch

IN Lai, Mu-Jen, Jungli, TAIWAN, PROVINCE OF CHINA
PA Chang, Chiung-Yu, Hsinchu, TAIWAN, PROVINCE OF CHINA
Vetra Technology, Inc., Hsinchu, TAIWAN, PROVINCE OF CHINA (non-U.S.
corporation)
PI US 6815722 B2 20041109
AI US 2003-601957 20030623 (10)
PRAI TW 2002-91136160 20021213
DT Utility
FS GRANTED
EXNAM Primary Examiner: Prenty, Mark V.
LREP Thomas, Kayden, Horstemeyer & Risley
CLMN Number of Claims: 9
ECL Exemplary Claim: 1
DRWN 3 Drawing Figure(s); 2 Drawing Page(s)
LN.CNT 404
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 27 OF 33 USPAT2 on STN

AB A method of forming a group-III nitride semiconductor **layer** on a light-emitting device. First, a **substrate** is provided. Next, a **buffer layer** is formed on the **substrate**. A hydrogen treatment is performed on the **buffer layer**. Finally, a group-III nitride semiconductor **layer** is formed on the **buffer layer**. According to the present invention, a hydrogen treatment is performed on the **buffer** to prevent corrosion during subsequent process and remove particles from the **buffer layer**. Thus, the structure of the **epitaxy layer** following formed on the **buffer layer** is enhanced.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:318803 USPAT2
TI Method of forming group-III nitride semiconductor **layer** on a light-emitting device
IN Terashima, Kazutaka, Hsinchu, TAIWAN, PROVINCE OF CHINA
Lai, Mu-Jen, Chuagli, TAIWAN, PROVINCE OF CHINA
Chang, Chiung-Yu, Taichung, TAIWAN, PROVINCE OF CHINA
PA Vetra Technology, Inc., Hsinchu, TAIWAN, PROVINCE OF CHINA (non-U.S.
corporation)
PI US 6828169 B2 20041207
AI US 2003-463355 20030617 (10)
RLI Continuation-in-part of Ser. No. US 2002-62116, filed on 30 Jan 2002
PRAI TW 2002-91120763 20020911
DT Utility
FS GRANTED
EXNAM Primary Examiner: Nguyen, Tuan H.
LREP Thomas, Kayden, Horstemeyer & Risley
CLMN Number of Claims: 20
ECL Exemplary Claim: 1
DRWN 6 Drawing Figure(s); 3 Drawing Page(s)
LN.CNT 306
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 28 OF 33 USPAT2 on STN

AB A p-n junction-type compound semiconductor light-emitting device having a **substrate** formed of a **single crystal**, a **first barrier layer** provided on the **substrate**, and formed of a compound semiconductor of a first conduction type, a **light-emitting layer** provided on the **first barrier layer** and formed of an indium (In)-containing group III nitride semiconductor of a first or a second conduction type, and an **evaporation-preventing layer** provided on the **light-emitting layer** for preventing the evaporation of indium from the **light-emitting layer**. The **evaporation-preventing layer** is formed of an undoped boron phosphide (BP)-base semiconductor of a second conduction type. A method for producing the **semiconductor-light emitting device** is also disclosed.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:255589 USPAT2
TI P-n junction-type compound semiconductor light-emitting device, production method thereof, lamp and light source
IN Udagawa, Takashi, Saitama, JAPAN
PA Showa Denko Kabushiki Kaisha, Tokyo, JAPAN (non-U.S. corporation)
PI US 6831293 B2 20041214
AI US 2003-389904 20030318 (10)
PRAI JP 2002-75297 20020319
US 2002-384095P 20020531 (60)
DT Utility
FS GRANTED
EXNAM Primary Examiner: Mai, Anh Duy
LREP Sughrue Mion, PLLC
CLMN Number of Claims: 13
ECL Exemplary Claim: 1
DRWN 7 Drawing Figure(s); 4 Drawing Page(s)
LN.CNT 965
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 29 OF 33 USPAT2 on STN

AB A pn-junction type compound semiconductor light-emitting device having a **substrate** formed of a **crystal**, a **first barrier layer** provided on the **substrate** and formed of an undoped **boron phosphide**-base semiconductor of **first conduction type**, and a **light-emitting layer** of a **first** or a **second conduction type** provided on the **first barrier layer** including a plurality of superposed constituent **layers** formed of group III nitride semiconductors each having a different band gap. The constituent **layer** of the **light-emitting layer** provided closest to the **first barrier layer** is a **first** light-emitting constituent **layer** formed of a group III nitride semiconductor containing phosphorus (P). A method for producing the semiconductor light-emitting device is also disclosed.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:248793 USPAT2
TI Pn-junction type compound semiconductor light-emitting device, production method thereof and white light-emitting diode
IN Udagawa, Takashi, Saitama, JAPAN
PA Showa Denko Kabushiki Kaisha, Tokyo, JAPAN (non-U.S. corporation)
PI US 6774402 B2 20040810
AI US 2003-384666 20030311 (10)
PRAI JP 2002-67473 20020312
US 2002-430648P 20021204 (60)
DT Utility
FS GRANTED
EXNAM Primary Examiner: Crane, Sara
LREP Sughrue Mion, PLLC
CLMN Number of Claims: 13
ECL Exemplary Claim: 1
DRWN 6 Drawing Figure(s); 3 Drawing Page(s)
LN.CNT 1246
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 30 OF 33 USPAT2 on STN

AB A pn-junction-type semiconductor light-emitting device having a **single-crystal silicon (Si) substrate** of **first conduction type**; a **first boron-phosphide-based semiconductor layer** of **first conduction type** provided on the **substrate**; a **light-emitting layer** formed of a Group III-V semiconductor **layer** of **first** or **second conduction type** which is doped with an element belonging to Group IV of the periodic table provided on the **first boron-phosphide-based semiconductor layer**; and **second boron-phosphide-based semiconductor layer** of **second conduction type** formed of a **boron-phosphide-based semiconductor**

layer of second conduction type containing a Group IV element provided on the light-emitting layer. The first boron-phosphide-based semiconductor layer, the light-emitting layer, and the second boron-phosphide-based semiconductor layer form a pn-junction-type hetero structure. In addition, the second conduction type is opposite the first conduction type. Also, disclosed is a method for producing the device.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:230061 USPAT2
TI P-n junction type **boron phosphide**-based semiconductor light-emitting device and production method thereof
IN Udagawa, Takashi, Saitama, JAPAN
PA Showa Denko Kabushiki Kaisha, Tokyo, JAPAN (non-U.S. corporation)
PI US 6831304 B2 20041214
AI US 2003-370761 20030224 (10)
PRAI JP 2002-47457 20020225
US 2002-367702P 20020328 (60)

DT Utility

FS GRANTED

EXNAM Primary Examiner: Thomas, Tom; Assistant Examiner: Lee, Eugene

LREP Sughrue Mion, PLLC

CLMN Number of Claims: 12

ECL Exemplary Claim: 1

DRWN 4 Drawing Figure(s); 2 Drawing Page(s)

LN.CNT 1268

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L12 ANSWER 31 OF 33 USPAT2 on STN

AB A **boron-phosphide**-based semiconductor light-emitting device having a semiconductor **substrate** of a first conduction type having, on its bottom surface, a bottom electrode; a **first boron-phosphide**-based semiconductor **layer** of a **first** conductive type provided on the **substrate**; a **Group III-V compound semiconductor active layer** provided on the **first boron-phosphide**-based semiconductor **layer**; a **second boron-phosphide**-based semiconductor **layer** of **second** conduction type provided on the **active layer**; and a top electrode provided on the surface of the **second boron-phosphide**-based semiconductor **layer**. The top electrode includes a lower electrode and an upper electrode, the lower electrode is in direct contact with the **second boron-phosphide**-based semiconductor **layer** and formed of a metal incapable of establishing ohmic contact with the **second boron-phosphide**-based semiconductor **layer**, and the upper electrode is provided on the lower electrode and formed of a metal capable of establishing ohmic contact with the **second boron-phosphide**-based semiconductor **layer**.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:205162 USPAT2
TI **Boron phosphide**-based semiconductor light-emitting device, production method thereof, and light-emitting diode
IN Udagawa, Takashi, Saitama, JAPAN
PA Showa Denko Kabushiki Kaisha, Tokyo, JAPAN (non-U.S. corporation)
PI US 6730941 B2 20040504
AI US 2003-353006 20030129 (10)
PRAI JP 2002-20824 20020130
US 2002-384097P 20020531 (60)

DT Utility

FS GRANTED

EXNAM Primary Examiner: Hu, Shouxiang

LREP Sughrue Mion, PLLC

CLMN Number of Claims: 15

ECL Exemplary Claim: 1

DRWN 6 Drawing Figure(s); 3 Drawing Page(s)

L12 ANSWER 32 OF 33 USPAT2 on STN

AB A stacked layer structure including a single crystal substrate; an amorphous or polycrystalline buffer layer formed from a boron-containing Group III-V compound semiconductor. The buffer layer is provided on the substrate; a cladding layer formed from a boron-containing Group III-V compound semiconductor is provided on the buffer layer; and a light-emitting layer having a quantum well structure including a barrier layer formed from a boron-containing Group III-V compound semiconductor and a well layer formed from a Group III nitride semiconductor is provided on the cladding layer. The barrier layer is formed from a boron-containing Group III-V compound semiconductor having the same lattice constant as a boron-containing Group III-V compound semiconductor constituting the cladding layer.

AN 2003:37454 USPAT2

TI Stacked layer structure, light-emitting device, lamp, and light source unit

IN Udagawa, Takashi, Saitama, JAPAN

PA Showa Denko Kabushiki Kaisha, Tokyo, JAPAN (non-U.S. corporation)

PI US 6835962 B2 20041228

AI US 2002-207901 20020731 (10)

PRAI JP 2001-233428 20010801

JP 2001-235454 20010802

JP 2001-247523 20010817

US 2001-323084P 20010919 (60)

US 2001-311103P 20010810 (60)

US 2001-311073P 20010810 (60)

DT Utility

FS GRANTED

EXNAM Primary Examiner: Jackson, Jerome

LREP Sughrue Mion, PLLC

CLMN Number of Claims: 13

ECL Exemplary Claim: 1

DRWN 6 Drawing Figure(s); 3 Drawing Page(s)

LN.CNT 1162

L12 ANSWER 33 OF 33 USPAT2 on STN

AB UV reflectors incorporated in UV LED-based light sources reduce the amount of UV radiation emission into the surroundings and increase the efficiency of such light sources. UV reflectors are made of nanometer-sized particles having a mean particle diameter less than about one-tenth of the wavelength of the UV light emitted by the UV LED, dispersed in a molding or casting material surrounding the LED. Other UV reflectors are series of layers of materials having alternating high and low refractive indices; each layer has a physical thickness of one quarter of the wavelength divided by the refractive index of the material. Nanometer-sized textures formed on a surface of the multilayered reflector further reduce the emission of UV radiation into the surroundings. UV LED-based light sources include such a multilayered reflector disposed on an encapsulating structure of a transparent material around a UV LED, particles of a UV-exitable phosphor dispersed in the transparent material. Alternatively, the transparent material also includes nanometer-sized particles of a UV-radiation scattering material.

CAS INDEXING IS AVAILABLE FOR THIS PATENT..

AN 2002:320216 USPAT2

TI UV reflectors and UV-based light sources having reduced UV radiation leakage incorporating the same

IN McNulty, Thomas Francis, Ballston Lake, NY, United States

Doxsee, Daniel Darcy, Sagamore Hills, OH, United States

Rose, James Wilson, Guilderland, NY, United States

PA General Electric Company, Niskayuna, NY, United States (U.S.)

PI corporation)
US 6686676 B2 20040203
AI US 2001-681560 20010430 (9)
DT Utility
FS GRANTED
EXNAM Primary Examiner: O'Shea, Sandra; Assistant Examiner: Macchiarolo, Peter
LREP Vo, Toan P., Patnode, Patrick K.
CLMN Number of Claims: 53
ECL Exemplary Claim: 1
DRWN 7 Drawing Figure(s); 7 Drawing Page(s)
LN.CNT 958
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

=> d his

(FILE 'HOME' ENTERED AT 13:08:07 ON 26 APR 2005)

FILE 'HCAPLUS, INSPEC, INPADOC, ABI-INFORM, USPATFULL, USPAT2' ENTERED AT
13:09:47 ON 26 APR 2005

L1 3474450 S (EPITAX? OR CRYSTAL?)
L2 58723 S (GAN OR GALLIUM(W) NITRIDE)
L3 2251103 S (SUBSTRATE#)
L4 280196 S (SINGLE(W) CRYSTAL OR MONO(W) CRYSTAL#)
L5 11 S (BORON(W) PHOSPHITE(W) BUFFER# OR BORON(W) PHOSPHITE)
L6 3603318 S (LAYER#)
L7 322468 S (FIRST OR PRIMARY) (4A) LAYER)
L8 290705 S (SECOND?) (4A) (LAYER)
L9 3 S L4 AND L5
L10 1246 S L1 AND L2 AND L3 AND L4 AND L6 AND L7 AND L8
L11 1188 S (BORON(W) PHOSPHIDE(W) BUFFER# OR BORON(W) PHOSPHIDE)
L12 33 S L10 AND L11

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